Date Filed: 9/19/2003

Express Mail: EV355345772US
Date of Deposit: September 19, 2003

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO.: YOR920030403US1	SERIAL NO.: CONFIRMATION NO. 10/666,353
	APPLICANT: Chandramouli Visweswariah	
(Use several sheets if necessary)	FILING DATE: ~~HEREWITH~~ 9/19/03	GROUP: 2825

REFERENCE DESIGNATION — U.S. PATENT DOCUMENTS

EXAMINER INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AH							

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

/PK/	AJ	Statistical Timing of Parametric Yield Prediction of Digital Integrated Circuits, by J.A.G. Jess, K. Kalafala, S.R. Naidu, R.H.J.M. Otten, C. Visweswariah, pp. 932-937, Design Automation Conference 2003
/PK/	AJ	Fast Statistical Timing Analysis By Probabilistic Event Propagation, by Jing-Jia Liou, Kwang-Ting Cheng, Sandip Kundu, and Angela Krstic, pp. 661-666, Design Automation Conference 2001
/PK/	AK	Explicit Computation of Performance as a Function of Process Variation by Lou Scheffer, TAU '02, pp. 1-8 , 2002.
/PK/	AL	Timing Yield Estimation from Static Timing Analysis, by Anne Gattiker, Sani Nassif, Rashmi Dinakar, and Chris Long, pp. 437-442, International Symposium on Quality Electronic Design, 2001.
/PK/	AM	J. A. G. Jess and C. Visweswariah, "System and method for statistical modeling and statistical analysis of integrated circuits," U.S. Patent Application number 10/184,329 filed with the U.S. Patent Office on June 27, 2002.

EXAMINER	/Phallaka Kik/	DATE CONSIDERED	12/01/2007

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Date Filed: 9/11/2007

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of ~~1~~ 2

Complete if Known	
Application Number	10/666,353
Filing Date	09/19/2003
First Named Inventor	Chandramouli Visweswariah
Art Unit	~~2841~~ 2825
Examiner Name	P. Kik
Attorney Docket Number	YOR920030403US1

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-			
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code[5] (if known)	Publication Date MM-DD-YYYY	~~Name of Patentee or Applicant of Cited Document~~ Translation	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T[6]
/PK/		~~PUPA~~JP-2002-279012	09/27/2002	Abstract only		Country
/PK/		~~PUPA04-274567~~JP-04-274567	09/30/1992	Abstract only		Japan
						Japan

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet	2	of	2

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Art Unit	~~2841~~ 2825
Examiner Name	P. Kik
Attorney Docket Number	YOR920030403US1

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/PK/		Jess, J.A.G. et al. "Statistical Timing for Parametric Yield Prediction of Digital Integrated Circuits", Proc. Design Automation Conference, ACM,P.932-937, 2-6 June 2003.	
/PK/		Nishimoto Shuji et al., "A Statistical Static Timing Analyzer for CMOS Combinatorial Circuits Considering Correlations Between Delays", Vol.100, No.475 ~~(2000/11/20)~~pp.11-16 , 23 November 2000, English translation of abstract only.	

Examiner Signature	/Phallaka Kik/	Date Considered	12/01/2007

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